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10/829,559	04/22/2004	Asher Hazanchuk	ALT.P030 (A1252)	6357

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EXAMINER	
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ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,559	HAZANCHUK ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 and 5-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 09/02/2008.

2. Claims 1, 3 and 5-22 are pending in this application. Claims 1, 11, 17 and 21-11 are independent claims. In Amendment, claims 2 and 4 are cancelled previously. This Office Action is made non-final after a RCE filed 09/02/2008.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3 and 5-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Re claim 1, the limitation "without utilizing a digital signal processor (DSP) capable of multiplying a number of bits forming the first and second numbers" is not clearly or directly supported or addressed in the original specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The applicant points for paragraphs [0005] and [0028-0047] for the support of this limitation however the examiner is unable to

correlate the cited paragraph with the amended/submitted limitation directly. Claims 11, 17 and 21-22 have the similar rejection as above.

Thus, claims 3, 5-10, 12-16 and 18-20 are also rejected for being dependent on the rejected base claims 1, 11 and 17.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1, 3 and 5-22 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 3 and 5-22 cite a method and device for performing multiplication in accordance with a predetermined mathematical algorithm. However, claims 1, 3 and 5-22 merely disclose series of steps for performing sum of shift products without providing a practical application. In addition, claims 1, 3, and 5-22 appear to preempt every substantial practical application of the idea embodied by the claims. The method claims 1, 3, 5-16 and 21 must also tight or direct to another statutory class as hardware for realizing the implementation. Therefore, claims 1, 3 and 5-22 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1, 3, 5-7, 9 and 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhandal et al. (U.S. 6,711,602) in view of Schier et al. (U.S. 7,046,723).

Re claim 1, Bhandal et al. disclose in Figures 1-22 a method for performing multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture of multiplier) without utilizing a DSP capable of multiplying a number of bits forming the first and second numbers (e.g. Figure 11B), comprising: generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B wherein SRC1_L as B is multiplying with SRC2_L as D by B*D) using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits then those forming the first and second numbers (e.g. by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands); a product of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B wherein SRC1_H as A is multiplying with SRC2_H as C by A*C); scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8) and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8); and summing a scaled product and a sealed stored value to generate a value representing a product of the first number and the second

number (e.g. output of adder 820 in Figure 8 and Figure 11B), wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits (e.g. Figure 11B wherein each of input operands consist of 32 bits and each of input multiplied operand is 16 bits).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 3, Bhandal et al. further disclose in Figures 1-22 the DSP block is configured to multiply two numbers of equal bit length (e.g. 16 bits by 16 bits in Figure 11B).

Re claim 5, Bhandal et al. further disclose in Figures 1-22 scaling the product comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 8 and 11B).

Re claim 6, Bhandal et al. further disclose in Figures 1-22 scaling the stored value comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 8 and 11B).

Re claim 7, Bhandal et al. fail to disclose in Figures 1-22 retrieving a second stored value designated as a product era third plurality of bits from the first number and a third plurality of bits from the second number; retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number; scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number and scaling the third stored value with respect to a position of the fourth plurality orbits from the first number and a position of the fourth plurality of bits from the second number, and summing a scaled second stored value and a scaled third stored value. However, Schier et al.'s disclose in Figures 1-4 retrieving a second stored value designated as a product of a third plurality of bits from the first number and a third plurality of bits from the second number (e.g. b2x in Figure 1); retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number (e.g. b3x in Figure 1); scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number (e.g. bit shift left in Figures 2-4) and scaling the third stored value with respect to a position of the fourth plurality of bits from the first number and a position of the fourth plurality of bits

from the second number (e.g. bit shift left in Figures 2-4), and summing a scaled second stored value and a scaled third stored value (e.g. output of adder 3 in Figure 1).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to retrieving a second stored value designated as a product era third plurality of bits from the first number and a third plurality of bits from the second number; retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number; scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number and scaling the third stored value with respect to a position of the fourth plurality orbits from the first number and a position of the fourth plurality of bits from the second number, and summing a scaled second stored value and a scaled third stored value as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 4 lines 3-21).

Re claim 9, it has similar limitations cited in claim 7. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 11, Bhandal et al. disclose in Figures 1-22 a method for implementing a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) without utilizing a DSP capable of multiplying a number of bits forming the first and second numbers (e.g. Figure 11B), comprising: configuring a digital signal processor (DSP) to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure

11B with product B*D); products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B with product A*C); routing an output from the DSP to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8), routing an output as second product to the adder (e.g. adder 820 in Figure 8) such that the output is scaled according to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8), and outputting a value representing a product of the second number where the first and second number each have more than the first plurality of bits (e.g. output of adder 820 in Figure 8), wherein the DSP is configured to support multiplication of no more than the first plurality of bits (e.g. 16 bits by 16 bits).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 12, it has similar limitations cited in claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, Bhandal et al. further disclose in Figures 1-22 configuring the DSP comprises determining a number of bits that the DSP will multiply (e.g. Figure 11B).

Re claim 14, Bhandal et al. further disclose in Figures 1-22 determining a number of the second plurality of bits from the first number and a number of the second plurality of bits from the second number (e.g. Figure 11B).

Re claim 15, Bhandal et al. further disclose in Figures 1-22 routing the output from the DSP has the effect of shifting the output from the DSP to a more significant bit position (e.g. left shifting 810 in Figure 8).

Re claim 16, Bhandal et al. fail to disclose in Figures 1-22 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position. However, Schier et al. disclose in Figures 1-4 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position (e.g. by bit shift left in Figures 2-4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 17, Bhandal et al. disclose in Figures 1-22 a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as

general architecture) without utilizing a DSP capable of multiplying a number of bits forming the first and second numbers (e.g. Figure 11B), comprising: a digital signal processor (DSP) configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B to produce B*D); a product resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B to produce A*C); and an adder that sums (e.g. by adder 820 in Figure 8) a scaled output of the DSP and a scaled output of the second product to output a value representing a product of the first and second number where the first and second number each have more than the first plurality of bits (e.g. by shifters 810 and 811 respectively), wherein the DSP is only configurable to support multiplication of a number of bits equal to or less than the first plurality of bits (e.g. multiplier performs 16 by 16 bits).

Bhandal et al. fail to disclose the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 18, Bhandal et al. fail to disclose in Figures 1-22 the DSP, the memory, and the adder reside on a field programmable gate array. However, Schier et al. disclose

in Figures 1-4 the DSP, the memory, and the adder reside on a field programmable gate array (e.g. abstract).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the DSP, the memory, and the adder reside on a field programmable gate array as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 19, it has similar limitations cited in claim 7. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 20, Bhandal et al. further disclose in Figures 1-22 the adder sums a sealed output of the second memory with the scaled output of the DSP and the scaled output of the memory (e.g. by adder 820 or adder 3).

Re claim 21, Bhandal et al. disclose in Figures 1-22 a method for implementing a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) without utilizing a DSP capable of multiplying a number of bits forming the first and second numbers (e.g. Figure 11B), comprising: configuring a digital signal processor (DSP) to perform multiplication on a first n bits from a first number and a first n bits from a second number (e.g. by product B*D in Figure 11B); products resulting from multiplication of a second m bits from the first number and a second m bits from the second number (e.g. by product A*C in Figure 11B); routing an output from the DSP to an adder (e.g. adder 820 in Figure 8) such that the output from the DSP is scaled according to a position of the first n bits from the first

number and a position of the first n bits from the second number (e.g. by shifter 810 in Figure 8); routing an output of the second product to the adder such that the output from the memory is scaled according to a position of the second m bits from the first number and a position of the second m bits from the second number (e.g. by shifter 811 in Figure 8); and outputting a value representing a product of the first and second number where the first and second number each have at least n + m number of bits (e.g. output of adder 820 in Figure 8 and Figure 11B).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 22, Bhandal et al. disclose in Figures 1-22 a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) without utilizing a DSP capable of multiplying a number of bits forming the first and second numbers (e.g. Figure 11B), comprising: a digital signal processor (DSP) configured to perform n*n multiplication on a first plurality of bits from

a first number and a first plurality of bits from a second number (e.g. produce B*D in Figure 11B with 16x16 bits multiplication); products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. produce A*C in Figure 11B with 16x16 bits multiplication); and an adder that sums a scaled output of the DSP and a scaled (e.g. scaling by shifters 810 and 811 in Figure 8) output of the memory to output a value representing a product of the first and second number (e.g. by adder 820 in Figure 8) where the first and second number each have more than n bits (e.g. each have 32 bits or 2n total in Figure 11B).

Bhandal et al. fail to disclose the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Response to Amendment

9. The amendment filed 09/02/2008 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Re claim 1, 11, 17 and 21-22, the applicant added the new limitation "without utilizing a digital signal processor (DSP) capable of multiplying a number of bits forming the first and second numbers" which is not clearly or directly supported or addressed in the original specification.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

10. Applicant's arguments filed 09/02/2008 have been fully considered but they are not persuasive.

a. The applicant argues in page 8 first paragraph for claims rejected under 35 U.S.C. 101 that the claims direct to a multiplier without having to utilize a DSP capable of multiplying a number of bits forming the two numbers.

The examiner respectfully submits that the new limitation is considered as new matter since it does not directly addressed in the original specification. Thus, the rejection under 101 is still valid and maintained. In addition, the method claims must also include or tight to another statutory class as hardware for realizing the implementation of the multiplier as addressed above.

b. The applicant argues in pages 9-11 for claims that the primary reference by Bhandal fails to disclose a multiplier that is configured to perform multiplication on all the number of bits used for forming the first second numbers being multiplied, and is not using a multiplier that is configured to perform multiplication on a fewer number of bits

than those forming the first and second numbers. In addition, the Schier teaches away from combining a DSP multiplier such as described in Bhandal.

The examiner respectfully submits that the above alleged limitations is clearly seen directly in Figures 11B or 11D by Bhandal wherein the multiplication is performed to multiply source 1 with source 2 but producing only half of the size of the actual bits of the multiplication. Thus, Figure 11B or 11D clearly meets the claim language. For the combination, neither Bhandal nor Schier discloses explicitly that it cannot be combined with other reference to form the claimed invention.

c. The applicant extensively argues in pages 11 and 15-16 that the secondary reference by Schier teaches away from combining the reference by "the performance of the digial...or FPGA".

The examiner respectfully submits that this specific paragraph does not teach anything about not combining the references as alleged by the applicant, but rather it states that the "performance" of any digital filter is depending on the architecture for implementation wherein the implementation comprises DSP, ASIC, or FPGA, and so on. Thus, it has nothing to do with specific combining the references or concepts.

d. The applicant argues in pages 12-13 that the invention by Schier does not require or permit the shifting which the Office is requiring for the "stored value" by shifter 811 in Figure 8 of Bhandal since the shifting would render the result incorrectly.

The examiner respectfully submits that the previous Office action already stated clearly that the secondary reference does not need to show every limitation cited in the primary reference. Thus, the examiner only borrows or applied the feature or limitation from the secondary reference by Schier of having the second product from a memory as clearly addressed in the rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

November 9, 2008

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	10/829,559	HAZANCHUK ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	